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EXAMINER	
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ART UNIT	PAPER NUMBER
2143	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/862,941	FLOOD ET AL.	
	Examiner	Art Unit	
	Kyung H. Shin	2143	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 October 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 3-53* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 3-53* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119.

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This action is responding to application papers dated 5/22/2001.

2. Claims **1, 3-53** are pending. Claim **3** has been amended. Claim **2** has been canceled. Independent claims are **1, 38, 39 and 52**.

Response to Arguments

3. Applicant's arguments filed 10/5/2007 have been fully considered but they are not persuasive.

3.1 Applicant argues that the referenced prior art does not disclose, "operational as both a master and a slave", (see Remarks Pages 10-11).

Examiner still insists that there is no disclosure for a synchronization apparatus that operates as both a master and a slave at the same time. Applicant has previously amended claim 1 with the limitation, *" the time synchronization apparatus is configurable to operate as **both** a synchronization master and a synchronization slave "*. There is *no disclosure within the specification or original claims* for this limitation. See USC 112, 1st paragraph rejection.

3.2 Applicant argues that the referenced prior art does not disclose, "failed to identify which feature of Yamanaka is the synchronization apparatus".. (see Remarks Page 12)

The Office Action discloses the limitations the Yamanaka prior art addresses.

3.3 Applicant argues, "combination discloses an inoperative device", (see Remarks

Page 11); "network transmission speeds", (see Remarks Page 13).

Applicant admits that the speed of the network is the determining factor to consider the apparatus seemingly inoperative. Voth discloses a time synchronization system utilizing UNIX type system. The dedicated processor utilized within the time synchronization system is loaded only with the required operating system features. The communications network utilized is a very high speed capable network and the communications speeds in the communications network are within the invention's specification. Therefore, these features (i.e. high speed communications, operating system loaded only with required features) make the prior art disclosure of the invention possible and operable. (see Voth col. 4, lines 19-21: high speed network)

3.4 Applicant argues that the referenced prior art does not disclose, "synchronization device is configurable", (see Remarks Page 12); "a synchronization circuit ... configurable by the host" (see Remarks Page 12); "configurable to operate as both a synchronization master and a synchronization slave" (see Remarks Page 12); "mutually exclusive scenarios". (see Remarks Page 12); "a time synchronization apparatus that is configurable". (see Remarks Page 12).

Yamanaka and Voth combination discloses a synchronization master that is configurable as per claim limitation. (see Yamanaka Figure 3A; Figure 3B; col. 1, lines 15-22; col. 2, lines 29-37; Figure 3A; col. 5, lines 5-9: configurable to operate as a master; Figure 3B; col. 5, lines 12-18: configurable to operate as a slave) In addition, Voth discloses that a synchronization apparatus can be configured as a master or as a

slave. (see Voth col. 4, lines 35-42)

3.5 Applicant argues that the referenced prior art does not disclose, "fixed time period for message transmission", (see Remarks Page 13); "fixed value for least common multiple (LCM)", (see Remarks Page 13)

Applicant

Applicant's invention discloses that a message is transmitted every 50μs which is a fixed time period. Voth discloses that the update period is performed at a regular or periodic fixed time period which can be equal to 50μs or some other time period a fixed time period for the transmission of messages. (see Voth col. 4, lines 43-54: update period is performed at a regular or periodic fixed time period which can be equal to 50us or some other time period). In addition, Voth discloses a least common multiple (LCM) or update cycle period. (see Voth col. 4, lines 43-54: "*...use a repeating update cycle...Update cycle...includes an initial calculation...scheduling period...a time adjustment period.*" Applicant's specification status on page 13 at lines 20-26 that "*...600ms is exemplary... other LCM periods fall within the scope of the present invention...*" Thus, LCM is equal to periodic update cycle.)

Examiner is not changing the claim language. The claimed limitation is for a message transmission frequency based on a fixed time interval. Voth discloses a fixed time interval for message transmission.

3.6 Applicant argues that the referenced prior art does not disclose, "time zones". (see Remarks Page 14)

A time synchronization apparatus has as its basis a time parameter which is principally the current time value for a computer system within a particular time zone. Voth discloses a time synchronization apparatus operational within a distributed computer systems operational over the Internet (a global interconnected network with multiple time zones).

3.7 Applicant argues, "obviousness rejection", (see Remarks Page 14).

The rejection to each independent and dependent claim includes a citation from the referenced prior art that discloses the basis for the rejection. Each obviousness combination clearly indicates the claim limitation the combined reference prior art teaches. In addition, a cited passage from the referenced prior art clearly indicates the motivation for the obviousness combination. Each obviousness combination's disclosure is equivalent to the Applicant's claimed limitation(s) for the claimed invention.

Achieved advantage is a valid motivation for the combination of referenced prior art. The combination of each referenced prior art combination states a motivation for the combination, which translates to an achieved advantage for the combination.

All of the referenced prior art is in the same field of endeavor and a search by one skilled in the art would have returned the referenced prior art within the set of returned prior art.

It is not a requirement that the referenced prior art solve the same problem as claimed invention in order to be combinable. There are three criteria for combination: (1) same file of endeavor; (2) motivation for the combination; and (3) successful

disclosure of claim limitation due to prior art combination.

Voth discloses a time synchronization system. (see Voth col. 2, lines 51-53: time synchronization system), the Rasmussen discloses a time synchronization system (see Rasmussen col. 4, lines 57-59; col. 12, lines 31-35), and Kuribayashi discloses a time synchronization system. Applicant's invention discloses a time synchronization apparatus. Therefore, the set of referenced prior art is analogous art and legitimate prior art and is utilized to disclose the applicant's invention.

A search of applicant's invention field of endeavor would have revealed a set of prior art including the referenced prior art. Motivation is provided within the Office Action for each combination. The combination of the indicated referenced prior art successfully discloses the indicated claim limitations and the claimed invention.

3.8 Applicant argues, "rejection of dependent claims". (see Remarks Page 14)

Arguments for dependent claims are based upon above arguments for independent claims 1, 39. The successful responses to arguments for independent claims 1, 39, also successfully respond to the current arguments against the dependent claims 8-12, 29, 35-37, 47.

3.9 The examiner has considered the applicant's remarks concerning systems and methods for time synchronization of operations in a control system. Synchronization networks and devices are provided for transferring synchronization information between controllers in a distributed or localized control system, which is employed in order to allow operation of such controllers to be synchronized with respect to time. Also

disclosed are synchronization protocols and hardware apparatus employed in synchronizing control operations in a control system. Applicant's arguments have thus been fully analyzed and considered but they are not persuasive.

After an additional analysis of the applicant's invention, remarks, and a search of the available prior art, it was determined that the current set of prior art consisting of Yamanaka (4,807,259), Voth (6,199,169), Ramussen (6,449,732) and Kuribayashi (6,775,246) which disclose applicant's invention including disclosures in Remarks dated October 5, 2007.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claim **1** is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter, which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Applicant has amended claim 1 with the limitation, "*the time synchronization apparatus is configurable to operate as* ***both*** *a synchronization master and a synchronization slave* ". There is *no disclosure within the specification or original claims* for this limitation. There is disclosure for an apparatus to act as **either** a

master **or** a slave. But, there is no disclosure for an apparatus to act as **both** a master and a slave **at the same time** as the claim limitation states.

Appropriate action is required. If applicant feels there is disclosure for this claim limitation, please indicate the required citation for confirmation.

Claim Rejections 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. **Claims 1, 3 - 7, 13 - 28, 30 - 34, 38 - 46, 48 - 53** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Yamanaka et al.** (US Patent No. **4,807,259**) in view of **Voth** (US Patent No. **6,199,169**: System and method for synchronizing time across a computer cluster, Filed Dec. 15, 1998).

Regarding Claim 1, Yamanaka discloses a time synchronization apparatus for synchronizing operation of a first controller with that of a second controller in a control

system, the synchronization apparatus comprising:

- a processor interface for interfacing the synchronization apparatus with a host processor, the time synchronization apparatus is configurable to operate as **both** a synchronization master and a synchronization slave; (see Yamanaka Figure 3A; Figure 3B; col. 1, lines 15-22; col. 2, lines 29-37; Figure 3A; col. 5, lines 5-9: configurable to operate as a master; Figure 3B; col. 5, lines 12-18: configurable to operate as a slave)
- a timing system with a clock that maintains an indication of time according to information received from one of the network and the host processor. (see Yamanaka Figure 3A; Figure 3B; col. 4, lines 6-14; col. 6, lines 41-63)

Yamanaka discloses a low bandwidth modem circuit for network connections in the network receipt of synchronization information and data. This type of network affords limited communications bandwidth and a limited number of possible network configurations and topologies.

However, Voth discloses wherein:

- a transmitter adapted to transmit synchronization information and data to a network in the control system; (see Voth col. 2, lines 57-60)
- a receiver adapted to receive synchronization information and data from the network; (see Voth col. 2, lines 60-61)

It would have been obvious to one of ordinary skill in the art to modify Yamanaka as taught by Voth to enable the capability to network communications in

a variety of configurations. One of ordinary skill in the art would have been motivated to employ the teachings of Voth in order to enable the capability to network communications over a wide range of network configurations and topologies. (see Voth col. 2, lines 27-30: "*... Based on the preceding discussion, it is not hard to appreciate that a need exists for time synchronization systems that are suitable for use in networks where the ethernet simplification does not apply. ...* "; col. 2, lines 39-43: "*... Currently available time synchronization systems may also require the network to process large numbers of synchronization messages. A large number of synchronization messages steal network bandwidth from other computing tasks. ...* ")

Regarding Claim 3, Yamanaka discloses the time synchronization apparatus of claim 1, being configured to operate as a synchronization master, the synchronization apparatus is a hardware module coupled to the host processor. (see Yamanaka Figure 3A; Figure 3B; col. 1, lines 15-22; col. 2, lines 29-37; Figure 3A; col. 5, lines 5-9: configurable to operate as a master; Figure 3B; col. 5, lines 12-18: configurable to operate as a slave) And, Voth discloses wherein the transmitter periodically transmits message frames at a fixed period. (see Voth col. 4, lines 43-47: frames transmitted at a fixed interval)

It would have been obvious to one of ordinary skill in the art to modify Yamanaka as taught by Voth to enable the capability to be configured to operate as a synchronization master. One of ordinary skill in the art would have been motivated to

employ the teachings of Voth in order to enable the capability to network communications over a wide range of network configurations and topologies. (see Voth col. 2, lines 27-30; col. 2, lines 39-43)

Regarding Claims 4, 15, Voth discloses the time synchronization apparatus of claim 3, 14, wherein the fixed period is about 50μs. (According to Applicant's specification on page 28 at lines 15-16, it states, *"...the synchronization component can transmit (broadcast) a frame every 50μs or some other fixed time period."* see Voth col. 4, lines 43-54: where the reference states that the update period is performed at a regular or periodic fixed time period which can be equal to 50us or some other time period.)

It would have been obvious to one of ordinary skill in the art to modify Yamanaka as taught by Voth to enable the capability where a fixed period is about 50μs. One of ordinary skill in the art would have been motivated to employ the teachings of Voth in order to enable the capability to network communications over a wide range of network configurations and topologies. (see Voth col. 2, lines 27-30; col. 2, lines 39-43)

Regarding Claims 5, 16, Voth discloses the time synchronization apparatus of claim 3, 14, wherein the transmitter transmits a message frame having an LCM indicator at a least common multiple (LCM) interval. (see Voth col. 4, lines 43-54: *"...use a repeating update cycle...Update cycle...includes an initial calculation ... scheduling period...a time adjustment period."* Applicant's specification states on page 13 at lines 20-26 that *"...least common multiple (LCM) period, ...can be set to the lowest integer multiple of*

periodic tasks..." (i.e. set to 1) Thus, LCM is tied to reference's periodic update cycle.)

It would have been obvious to one of ordinary skill in the art to modify Yamanaka as taught by Voth to enable the capability to transmit a message frame having an LCM indicator. One of ordinary skill in the art would have been motivated to employ the teachings of Voth in order to enable the capability to network communications over a wide range of network configurations and topologies. (see Voth col. 2, lines 27-30; col. 2, lines 39-43)

Regarding Claims 6, 17, Voth discloses the time synchronization apparatus of claim 5, 16, wherein the LCM interval is 600ms. (see Voth col. 4, lines 43-54: *"...use a repeating update cycle...Update cycle...includes an initial calculation...scheduling period...a time adjustment period."* Applicant's specification status on page 13 at lines 20-26 that *"...600ms is exemplary... other LCM periods fall within the scope of the present invention..."* Thus, LCM is equal to periodic update cycle.)

It would have been obvious to one of ordinary skill in the art to modify Yamanaka as taught by Voth to enable the capability where the LCM interval is 600ms. One of ordinary skill in the art would have been motivated to employ the teachings of Voth in order to enable the capability to network communications over a wide range of network configurations and topologies. (see Voth col. 2, lines 27-30; col. 2, lines 39-43)

Regarding Claims 7, 30, Voth discloses the time synchronization apparatus of claim 3, 14, being configured as a synchronization master, wherein the transmitter transmits

message frames having multiplexed data and direct data. (see Voth col. 3, lines 1-9)

It would have been obvious to one of ordinary skill in the art to modify Yamanaka as taught by Voth to enable the capability to be configured as a synchronization master. One of ordinary skill in the art would have been motivated to employ the teachings of Voth in order to enable the capability to network communications over a wide range of network configurations and topologies. (see Voth col. 2, lines 27-30; col. 2, lines 39-43)

Regarding Claim 13, Voth discloses the time synchronization apparatus of claim 7, wherein the timing system is adjustable according to information received from the host processor. (see Voth col. 2, lines 51-54)

It would have been obvious to one of ordinary skill in the art to modify Yamanaka as taught by Voth to enable the capability where the timing system is adjustable. One of ordinary skill in the art would have been motivated to employ the teachings of Voth in order to enable the capability to network communications over a wide range of network configurations and topologies. (see Voth col. 2, lines 27-30; col. 2, lines 39-43)

Regarding Claim 14, Voth discloses the time synchronization apparatus of claim 1, being configured as a synchronization slave, wherein the receiver receives message frames at a fixed period, and wherein the timing system is adjusted according to the fixed period. (see Voth col. 4, lines 43-47)

It would have been obvious to one of ordinary skill in the art to modify Yamanaka

as taught by Voth to enable the capability to be configured as a synchronization slave. One of ordinary skill in the art would have been motivated to employ the teachings of Voth in order to enable the capability to network communications over a wide range of network configurations and topologies. (see Voth col. 2, lines 27-30; col. 2, lines 39-43)

Regarding Claim 18, Voth discloses the time synchronization apparatus of claim 16, wherein the timing system is adjusted according to the LCM indicator. (see Voth col. 4, lines 47-44)

It would have been obvious to one of ordinary skill in the art to modify Yamanaka as taught by Voth to enable the capability where the timing system is adjusted. One of ordinary skill in the art would have been motivated to employ the teachings of Voth in order to enable the capability to network communications over a wide range of network configurations and topologies. (see Voth col. 2, lines 27-30; col. 2, lines 39-43)

Regarding Claim 19, Voth discloses the time synchronization apparatus of claim 16, wherein the receiver interrupts the host processor according to the LCM indicator. (see Voth col. 4, lines 43-47)

It would have been obvious to one of ordinary skill in the art to modify Yamanaka as taught by Voth to enable the capability where the receiver interrupts the host processor. One of ordinary skill in the art would have been motivated to employ the teachings of Voth in order to enable the capability to network communications over a

wide range of network configurations and topologies. (see Voth col. 2, lines 27-30; col. 2, lines 39-43)

Regarding Claim 20, Voth discloses the time synchronization apparatus of claim 14, being configured to operate as a synchronization master, wherein the transmitter periodically transmits message frames at a fixed period. (see Voth col. 4, lines 43-47)

It would have been obvious to one of ordinary skill in the art to modify Yamanaka as taught by Voth to enable the capability to be configured to operate as a synchronization master. One of ordinary skill in the art would have been motivated to employ the teachings of Voth in order to enable the capability to network communications over a wide range of network configurations and topologies. (see Voth col. 2, lines 27-30; col. 2, lines 39-43)

Regarding Claim 21, Voth discloses the time synchronization apparatus of claim 20, wherein the message frames received and transmitted by the receiver and transmitter, respectively, comprise multiplexed data and direct data. (see Voth col. 5, lines 18-25)

It would have been obvious to one of ordinary skill in the art to modify Yamanaka as taught by Voth to enable the capability where the message frames received and transmitted comprise multiplexed data and direct data. One of ordinary skill in the art would have been motivated to employ the teachings of Voth in order to enable the capability to network communications over a wide range of network configurations and topologies. (see Voth col. 2, lines 27-30; col. 2, lines 39-43)

Regarding Claims 22, 43, Voth discloses the time synchronization apparatus of claim 21, 39, wherein the data field comprises 6 32-bit words, and wherein the amount of multiplexed data and the amount of direct data in each message frame is configurable. (see Voth col. 5, lines 50-59; col. 6, lines 10-14: *"Different implementations of the present invention may use difference sizes for an, or all, of these components."*, where reference states that different sizes and values (i.e. amounts of data: 32 bit words) can be used for the data contained within message frames and therefore is configured by implementation.)

It would have been obvious to one of ordinary skill in the art to modify Yamanaka as taught by Voth to enable the capability where the data field comprises 6 32-bit words. One of ordinary skill in the art would have been motivated to employ the teachings of Voth in order to enable the capability to network communications over a wide range of network configurations and topologies. (see Voth col. 2, lines 27-30; col. 2, lines 39-43)

Regarding Claim 23, Voth discloses the time synchronization apparatus of claim 22, wherein each message frame comprises a direct data portion and a multiplexed data portion, wherein the direct data comprises the direct data portion of a single frame, and wherein the multiplexed data comprises the multiplexed data portions of a plurality of frames. (see Voth col. 5, lines 18-25)

It would have been obvious to one of ordinary skill in the art to modify Yamanaka

as taught by Voth to enable the capability where each message frame comprises a direct data portion and a multiplexed data portion. One of ordinary skill in the art would have been motivated to employ the teachings of Voth in order to enable the capability to network communications over a wide range of network configurations and topologies. (see Voth col. 2, lines 27-30; col. 2, lines 39-43)

Regarding Claim 24, Voth discloses the time synchronization apparatus of claim 23, wherein the multiplexed data portion comprises configuration information indicative of the amount of multiplexed data and the amount of direct data in each message frame. (see Voth col. 5, lines 26-29; col. 5, lines 50-59)

It would have been obvious to one of ordinary skill in the art to modify Yamanaka as taught by Voth to enable the capability where the multiplexed data portion comprises configuration information. One of ordinary skill in the art would have been motivated to employ the teachings of Voth in order to enable the capability to network communications over a wide range of network configurations and topologies. (see Voth col. 2, lines 27-30; col. 2, lines 39-43)

Regarding Claims 25, 26, Voth discloses the time synchronization apparatus of claim 24, wherein the receiver presents direct data or multiplexed data from received message frames to the host processor at the fixed or a multiple of the fixed period. (see Voth col. 4, line 67 - col. 5, line 5)

It would have been obvious to one of ordinary skill in the art to modify Yamanaka

as taught by Voth to enable the capability where the receiver presents direct data or multiplexed data from received message frames to the host processor. One of ordinary skill in the art would have been motivated to employ the teachings of Voth in order to enable the capability to network communications over a wide range of network configurations and topologies. (see Voth col. 2, lines 27-30; col. 2, lines 39-43)

Regarding Claim 27, Voth discloses the time synchronization apparatus of claim 14, comprising a multiplier receiving an operand from the receiver, a multiplication value on the host processor, and providing a multiplication result value to at least one of the host processor and the transmitter, wherein the multiplication result value is the product of the multiplication value and the operand. (see Voth col. 5, lines 18-20)

It would have been obvious to one of ordinary skill in the art to modify Yamanaka as taught by Voth to enable the capability comprising a multiplier receiving an operand from the receiver. One of ordinary skill in the art would have been motivated to employ the teachings of Voth in order to enable the capability to network communications over a wide range of network configurations and topologies. (see Voth col. 2, lines 27-30; col. 2, lines 39-43)

Regarding Claims 28, 32, Voth discloses the time synchronization apparatus of claim 27, 30, wherein the direct data received in the message frame comprises the operand. (see Voth col. 5, lines 18-25)

It would have been obvious to one of ordinary skill in the art to modify Yamanaka

as taught by Voth to enable the capability where the direct data received in the message frame comprises the operand. One of ordinary skill in the art would have been motivated to employ the teachings of Voth in order to enable the capability to network communications over a wide range of network configurations and topologies. (see Voth col. 2, lines 27-30; col. 2, lines 39-43)

Regarding Claim 31, Voth discloses the time synchronization apparatus of claim 30, wherein at least a portion of the direct data in the message frames transmitted by the transmitter is provided to the transmitter by the receiver, wherein the direct data from a received message frame is passed through to the transmitter. (see Voth col. 6, lines 31-37)

It would have been obvious to one of ordinary skill in the art to modify Yamanaka as taught by Voth to enable the capability where at least a portion of the direct data in the message frames is provided to the transmitter by the receiver. One of ordinary skill in the art would have been motivated to employ the teachings of Voth in order to enable the capability to network communications over a wide range of network configurations and topologies. (see Voth col. 2, lines 27-30; col. 2, lines 39-43)

Regarding Claims 33, 34, Voth discloses the time synchronization apparatus of claim 30, wherein at least a portion of the direct data and multiplexed data in the message frames transmitted by the transmitter is provided to the transmitter by the host processor. (see Voth col. 5, lines 20-25)

It would have been obvious to one of ordinary skill in the art to modify Yamanaka as taught by Voth to enable the capability where at least a portion of the direct data and multiplexed data in the message frames is provided to the transmitter by the host processor. One of ordinary skill in the art would have been motivated to employ the teachings of Voth in order to enable the capability to network communications over a wide range of network configurations and topologies. (see Voth col. 2, lines 27-30; col. 2, lines 39-43)

Regarding Claim 38, Yamanaka discloses a synchronization module in a control chassis for synchronizing operation of a first controller in the control chassis with that of a second controller outside the control chassis, comprising:

- a host processor in communication with the first controller via a backplane bus in the control chassis; (see Figure 3A; Figure 3B; col. 1, lines 15-22; col. 2, lines 29-37)
- a synchronization circuit operatively associated with the host processor, the transmitter, the receiver, and the timing system, and configurable by the host processor to operate the module as one of a synchronization master and a synchronization slave. (see Figure 3A; col. 5, lines 5-9: configurable to operate as a master; Figure 3B; col. 5, lines 12-18: configurable to operate as a slave)

Yamanaka discloses a low bandwidth modem circuit for network connections in the network receipt of synchronization information and data. This type of network

affords limited communications bandwidth and a limited number of possible network configurations and topologies.

However, Voth discloses wherein:

- a transmitter adapted to transmit synchronization information and data to a network in the control system; (see Voth col. 2, lines 57-60)

- a receiver adapted to receive synchronization information and data from the network; (see Voth col. 2, lines 60-61)

- a timing system with a clock and maintaining an indication of time according to information received from one of the network and the host processor; (see Voth col. 2, lines 51-54)

It would have been obvious to one of ordinary skill in the art to modify Yamanaka as taught by Voth to enable the capability to network communications in a variety of configurations. One of ordinary skill in the art would have been motivated to employ the teachings of Voth in order to enable the capability to network communications over a wide range of network configurations and topologies. (see Voth col. 2, lines 27-30; col. 2, lines 39-43)

Regarding Claim 39, Yamanaka discloses a synchronization circuit for synchronizing operation of a first controller with that of a second controller in a control system, comprising:

- a processor interface for interfacing the synchronization circuit with a host processor; (see Yamanaka col. 1, lines 15-22; col. 2, lines 29-37)

- a timing system with a clock and maintaining an indication of time according to information received from one of the network and the host processor, wherein the synchronization circuit is configurable by the host processor to operate as one of a synchronization master and a synchronization slave. (see Yamanaka Figure 3A; col. 5, lines 5-9: configurable to operate as a master; Figure 3B; col. 5, lines 12-18: configurable to operate as a slave)

Yamanaka discloses a low bandwidth modem circuit for network connections in the network receipt of synchronization information and data. This type of network affords limited communications bandwidth and a limited number of possible network configurations and topologies.

However, Voth discloses wherein:

- a transmitter component adapted to transmit synchronization information and data to a network in the control system; (see Voth col. 2, lines 57-60)
- a receiver component adapted to receive synchronization information and data from the network; (see Voth col. 2, lines 60-61) and

It would have been obvious to one of ordinary skill in the art to modify Yamanaka as taught by Voth to enable the capability to network communications in a variety of configurations. One of ordinary skill in the art would have been motivated to employ the teachings of Voth in order to enable the capability to network communications over a wide range of network configurations and topologies. (see Voth col. 2, lines 27-30; col. 2, lines 39-43)

Regarding Claims 40, 41, Voth discloses the system of claim 39, wherein the transmitter component periodically transmits message frames comprising direct data, and wherein the direct data is obtained from at least one of the receiver, the host processor, and the multiplier. (see Voth col. 5, lines 18-25)

It would have been obvious to one of ordinary skill in the art to modify Yamanaka as taught by Voth to enable the capability where the transmitter component periodically transmits message frames. One of ordinary skill in the art would have been motivated to employ the teachings of Voth in order to enable the capability to network communications over a wide range of network configurations and topologies. (see Voth col. 2, lines 27-30; col. 2, lines 39-43)

Regarding Claim 42, Voth discloses the system of claim 39, wherein the transmitter component periodically transmits message frames comprising multiplexed data, and wherein the multiplexed data is obtained from the host processor. (see Voth col. 4, lines 43-47)

It would have been obvious to one of ordinary skill in the art to modify Yamanaka as taught by Voth to enable the capability where the transmitter component periodically transmits message frames comprising multiplexed data. One of ordinary skill in the art would have been motivated to employ the teachings of Voth in order to enable the capability to network communications over a wide range of network configurations and topologies. (see Voth col. 2, lines 27-30; col. 2, lines 39-43)

Regarding Claim 44, Voth discloses the system of claim 39, wherein the receiver component periodically receives message frames comprising direct data, multiplexed data, and status information from the network, and wherein the synchronization circuit provides at least one of received direct data, received multiplexed date and received status information from the receiver component to the host processor. (see Voth col. 6, lines 31-37)

It would have been obvious to one of ordinary skill in the art to modify Yamanaka as taught by Voth to enable the capability where the receiver component periodically receives message frames comprising direct data, multiplexed data, and status information. One of ordinary skill in the art would have been motivated to employ the teachings of Voth in order to enable the capability to network communications over a wide range of network configurations and topologies. (see Voth col. 2, lines 27-30; col. 2, lines 39-43)

Regarding Claim 45, Voth discloses the system of claim 44, further comprising a multiplier operating on the received direct data, and wherein the synchronization circuit provides a multiplier result value from the multiplier to the host processor. (see Voth col. 5, lines 18-20)

It would have been obvious to one of ordinary skill in the art to modify Yamanaka as taught by Voth to enable the capability comprising a multiplier operating on the received direct data. One of ordinary skill in the art would have been motivated to

employ the teachings of Voth in order to enable the capability to network communications over a wide range of network configurations and topologies. (see Voth col. 2, lines 27-30; col. 2, lines 39-43)

Regarding Claim 46, Voth discloses the system of claim 45, wherein the synchronization circuit provides a multiplication value to the multiplier from the host processor. (see Voth col. 5, lines 18-20)

It would have been obvious to one of ordinary skill in the art to modify Yamanaka as taught by Voth to enable the capability where the synchronization circuit provides a multiplication value to the multiplier. One of ordinary skill in the art would have been motivated to employ the teachings of Voth in order to enable the capability to network communications over a wide range of network configurations and topologies. (see Voth col. 2, lines 27-30; col. 2, lines 39-43)

Regarding Claim 48, Voth discloses the system of claim 39, wherein the transmitter component periodically transmits message frames comprising direct data, multiplexed data, and configuration information, and wherein the synchronization circuit provides at least one of the direct data, multiplexed data, and configuration information to the transmitter component from the host processor. (see Voth col. 5, lines 18-25)

It would have been obvious to one of ordinary skill in the art to modify Yamanaka as taught by Voth to enable the capability where the transmitter component periodically transmits message frames comprising direct data, multiplexed data, and configuration

information. One of ordinary skill in the art would have been motivated to employ the teachings of Voth in order to enable the capability to network communications over a wide range of network configurations and topologies. (see Voth col. 2, lines 27-30; col. 2, lines 39-43)

Regarding Claim 49, Voth discloses the system of claim 39, wherein the transmitter component periodically transmits message frames having synchronization information, wherein the synchronization information is obtained from the timing system, and wherein the timing system is adjusted according to at least one of synchronization information received from the network and synchronization information from the host processor. (see Voth col. 4, lines 43-47; col. 2, lines 51-54)

It would have been obvious to one of ordinary skill in the art to modify Yamanaka as taught by Voth to enable the capability where the transmitter component periodically transmits message frames having synchronization information. One of ordinary skill in the art would have been motivated to employ the teachings of Voth in order to enable the capability to network communications over a wide range of network configurations and topologies. (see Voth col. 2, lines 27-30; col. 2, lines 39-43)

Regarding Claim 50, Voth discloses the system of claim 39, wherein the synchronization circuit interrupts the host processor according to receipt of an LCM indicator by the receiver. (see Voth col. 4, lines 43-47)

It would have been obvious to one of ordinary skill in the art to modify Yamanaka

as taught by Voth to enable the capability where the synchronization circuit interrupts the host processor. One of ordinary skill in the art would have been motivated to employ the teachings of Voth in order to enable the capability to network communications over a wide range of network configurations and topologies. (see Voth col. 2, lines 27-30; col. 2, lines 39-43)

Regarding Claim 51, Voth discloses the system of claim 39, wherein the synchronization circuit interrupts the host processor periodically for presentation of at least one of direct data and multiplexed data from the receiver to the host processor. (see Voth col. 4, lines 43-47)

It would have been obvious to one of ordinary skill in the art to modify Yamanaka as taught by Voth to enable the capability where the synchronization circuit interrupts the host processor periodically. One of ordinary skill in the art would have been motivated to employ the teachings of Voth in order to enable the capability to network communications over a wide range of network configurations and topologies. (see Voth col. 2, lines 27-30; col. 2, lines 39-43)

Regarding Claim 52, Voth discloses a synchronization system for synchronizing a first controller with a second controller in a control system, comprising:

- means for interfacing the synchronization circuit with a host processor; (see Figure 3A; Figure 3B; col. 1, lines 15-22; col. 2, lines 29-37)
- means for maintaining an indication of time according to information received

from one of the network and the host processor, wherein the synchronization circuit is configurable by the host processor to operate as one of a synchronization master and a synchronization slave. (see Figure 3A; col. 5, lines 5-9: configurable to operate as a master; Figure 3B; col. 5, lines 12-18: configurable to operate as a slave)

Yamanaka discloses a low bandwidth modem circuit for network connections in the network receipt of synchronization information and data. This type of network affords limited communications bandwidth and a limited number of possible network configurations and topologies.

However, Voth discloses wherein:

- means for transmitting synchronization information and data to a network in the control system; (see Voth col. 2, lines 57-60)
- means for receiving synchronization information and data from the network; (see Voth col. 2, lines 60-61)

It would have been obvious to one of ordinary skill in the art to modify Yamanaka as taught by Voth to enable the capability to network communications in a variety of configurations. One of ordinary skill in the art would have been motivated to employ the teachings of Voth in order to enable the capability to network communications over a wide range of network configurations and topologies. (see Voth col. 2, lines 27-30; col. 2, lines 39-43)

Regarding Claims 53, Voth discloses the time synchronization apparatus of claim 1,

the synchronization apparatus exists in a different synchronization time zone from that of the host processor. (see Voth col. 4, lines 17-19: distributed internetworking environment such as the Internet operates across time zones)

It would have been obvious to one of ordinary skill in the art to modify Yamanaka as taught by Voth to enable the capability where the synchronization apparatus exists in a different synchronization time zone. One of ordinary skill in the art would have been motivated to employ the teachings of Voth in order to enable the capability to network communications over a wide range of network configurations and topologies. (see Voth col. 2, lines 27-30; col. 2, lines 39-43)

8. **Claims 8, 9, 10, 11, 12** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Yamanaka-Voth** and further in view of **Ramussen et al.** (US Patent No. **6,449,732**: Method and apparatus for processing control using a multiple redundant processor control system).

Regarding Claim 8, Voth discloses a header with flag bytes, a control byte and a data field and a bitmask used in error detection for data within the message frames. Voth does not disclose specifically the CRC technique in error detection procedures. However, Rasmussen discloses the time synchronization apparatus of claim 7, wherein the same comprises three flag bytes, a control byte, a data field comprising the multiplexed data and the direct data, and two CRC bytes. (see Rasmussen col. 14, lines 1-4: *"Calculates and check the received CRCs..."* ; col. 14, lines 16-19: *"Calculates and*

send the transmit CRCs...")

It would have been obvious to one of ordinary skill in the art to modify Yamanaka as taught by Voth to enable the capability for a header with flag bytes, a control byte and a data field and a bitmask used in error detection for data within the message frames, and to modify Yamanaka-Voth with the error detection capabilities as taught by Rasmussen. One of ordinary skill in the art would have been motivated to employ the teachings of Voth in order to enable the capability to network communications over a wide range of network configurations and topologies (see Voth col. 2, lines 27-30; col. 2, lines 39-43), and to employ the invention of Rasmussen in order to enhance the processing of time synchronization information with an extension in error detection capabilities (see Rasmussen col. 5, lines 24-27: *"...hardware loop-back fault detection, CRC checking...."*).

Regarding Claims 9, 12, Voth discloses the time synchronization apparatus of claim 8, wherein the data field comprises 6 32-bit words, and wherein the amount of multiplexed data and the amount of direct data in each message frame is configurable. (see Voth col. 5, lines 50-59; col. 6, lines 10-14: *"Different implementations of the present invention may use difference sizes for an, or all, of these components."*, where reference states that different sizes and values (i.e. amounts of data: 32 bit words) can be used for the data contained within message frames and therefore is configured by implementation.)

It would have been obvious to one of ordinary skill in the art to modify Yamanaka

as taught by Voth to enable the capability where the data field comprises 6 32-bit words. One of ordinary skill in the art would have been motivated to employ the teachings of Voth in order to enable the capability to network communications over a wide range of network configurations and topologies. (see Voth col. 2, lines 27-30; col. 2, lines 39-43)

Regarding Claim 10, Voth discloses the time synchronization apparatus of claim 9, wherein each message frame comprises a direct data portion and a multiplexed data portion, wherein the direct data comprises the direct data portion of a single frame, and wherein the multiplexed data comprises the multiplexed data portions of a plurality of frames. (see Voth col. 5, lines 18-25)

It would have been obvious to one of ordinary skill in the art to modify Yamanaka as taught by Voth to enable the capability where each message frame comprises a direct data portion and a multiplexed data portion. One of ordinary skill in the art would have been motivated to employ the teachings of Voth in order to enable the capability to network communications over a wide range of network configurations and topologies. (see Voth col. 2, lines 27-30; col. 2, lines 39-43)

Regarding Claim 11, Voth discloses the time synchronization apparatus of claim 10, wherein the multiplexed data portion comprises configuration information indicative of the amount of multiplexed data and the amount of direct data in each message frame. (see Voth col. 5, lines 26-32; col. 5, lines 48-59)

It would have been obvious to one of ordinary skill in the art to modify Yamanaka as taught by Voth to enable the capability where the multiplexed data portion comprises configuration information. One of ordinary skill in the art would have been motivated to employ the teachings of Voth in order to enable the capability to network communications over a wide range of network configurations and topologies. (see Voth col. 2, lines 27-30; col. 2, lines 39-43)

9. **Claims 29, 35, 36, 37, 47** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Yamanaka-Voth** and further in view of **Kuribayashi et al.** (US Patent No. **6,775,246**: Method of determining master and slaves by communication capability of network nodes).

Voth discloses a time synchronization apparatus with designated master and slave nodes and a timing system with a periodic and continuously updating feature. (see Voth col. 35, lines 45: *"... a distributed system that maintains the synchronization between time clocks ..., one of the nodes...assumes a master role. The remaining nodes 102 then function as slaves ...To synchronize time clocks 212, master node 102a and slave nodes 102b-d use a repeating update cycle ...."*)

Regarding Claims 29, 47, Voth does not disclose an apparatus to process status information from an upstream device. However, Kuribayashi discloses the time synchronization apparatus of claim 14, 44, wherein the message frame comprises a status component indicative of the status of an upstream device and error counter,

wherein the receiver provides the status component to the host processor. (see Kuribayashi col. 2, lines 9-19; col. 8, lines 37-42)

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Yamanaka-Voth with an apparatus to process status information from an upstream device as taught by Kuribayashi. One of ordinary skill in the art would be motivated to employ the invention of Kuribayashi in order to extend the processing of time synchronization information to control the operation of additional devices. (see Kuribayashi col. 1, lines 53-57: "*...provide a novel communication control apparatus, which permits the proper and simple setting of transmission/reception nodes...synchronization information in a high-speed network.*")

Regarding Claim 35, Voth does not disclose a procedure to process a status signal from an upstream device in a daisy-chain. However, Kuribayashi discloses the time synchronization apparatus of claim 1, being configured as an intermediate node in a daisy-chain topology, the receiver receiving synchronization information from an upstream device in the daisy-chain, and the transmitter transmitting the synchronization information to at least one downstream device in the daisy-chain. (see Kuribayashi col. 2, lines 9-19; col. 8, lines 37-42)

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Yamanaka-Voth in order for an apparatus to process status information from an upstream device as taught by Kuribayashi. One of ordinary skill in the art would be motivated to employ the invention of Kuribayashi in order to

extend the processing of time synchronization information controlling the operation of networked devices. (see Kuribayashi col. 1, lines 53-57: *"...provide a novel communication control apparatus, which permits the proper and simple setting of transmission/reception nodes ...synchronization information in a high-speed network."*)

Regarding Claim 36, Voth discloses the time synchronization apparatus of claim 35, wherein the receiver receives message frames at a fixed period, and wherein the transmitter transmits message frames at the fixed period comprising direct data and multiplexed data. (see Voth col. 4, lines 47-54)

It would have been obvious to one of ordinary skill in the art to modify Yamanaka as taught by Voth to enable the capability where the receiver receives message frames at a fixed period. One of ordinary skill in the art would have been motivated to employ the teachings of Voth in order to enable the capability to network communications over a wide range of network configurations and topologies. (see Voth col. 2, lines 27-30; col. 2, lines 39-43)

Regarding Claim 37, Voth discloses the time synchronization apparatus of claim 36, wherein at least a portion of the direct data in the message frames transmitted by the transmitter is provided to the transmitter by the receiver, wherein the direct data from a received message frame is passed through to the transmitter. (see Voth col. 4, lines 47-54)

It would have been obvious to one of ordinary skill in the art to modify Yamanaka

as taught by Voth to enable the capability where at least a portion of the direct data in the message frames transmitted by the transmitter is provided to the transmitter and the direct data from a received message frame is passed through to the transmitter. One of ordinary skill in the art would have been motivated to employ the teachings of Voth in order to enable the capability to network communications over a wide range of network configurations and topologies. (see Voth col. 2, lines 27-30; col. 2, lines 39-43)

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kyung H Shin whose telephone number is 703-305-

0711. The examiner can normally be reached on 9 am - 7 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David A Wiley can be reached on 703-308-5221. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

SUPERVISORY PATENT EXAMINER

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

K H S
Kyung H Shin
Patent Examiner
Art Unit 2143

KHS
December 10, 2007